Precision, 14-bit Pseudo Differential 300 kSPS SAR ADC

Features

- 14-bit pseudo differential, no missing code.
- Throughput: 300 kSPS
- INL: ± 0.25 LSB
- DNL: ± 0.25 LSB
- SINAD: 85 dB at 1 kHz
- THD: -103 dB at 1 kHz
- Pseudo differential input range: 0 V to V_{REF}
- No pipeline delay
- Single supply 5 V
- 1.8 V / 2.5 V / 3 V / 5 V logic interface
- Packages: MSOP-10 / DFN-10
- Standby current: 2 nA

Applications

- Precision data acquisition
- Automated testing
- Precision instrument
- Medical instrument

General Description

ZJC2017 is low noise, low power consumption, 14-bit pseudo differential SAR ADC with throughput up to 300 kSPS. The part is available in small package and easy to use. It can reduce the power consumption and complexity of the system, thus achieve high density designs.

ZJC2017 requires 5 V of power supply to sample the analog input voltage between IN+ and IN- ranging from 0 V to V_{REF} (V_{REF}: 0.5 V to V_{DD}). The reference voltage of ZJC2017 is provided externally, and can be set up to the supply voltage. Utilizing the independent VIO pin, ZJC2017 can be compatible with 1.8 V, 2.5 V, 3.3 V and 5 V logic interface. The part provides one SPI-compatible serial port and also supports daisy-chain operation for serial cascading of multiple devices.

ZJC2017 is available in 10-lead MSOP and DFN packages. The operating temperature is - 40 °C to +85 °C. ZJC2017 series is pin compatible with industry standard parts.

Typical Application

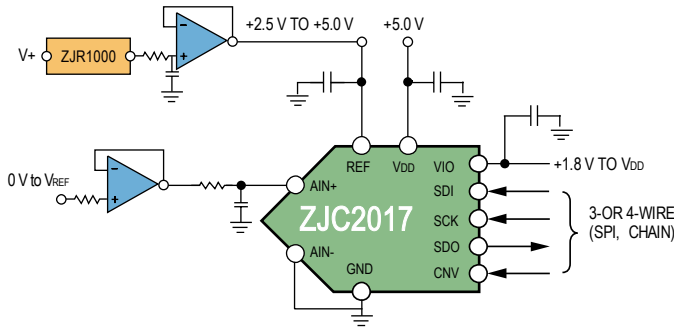

Figure 1. Application Examples

Typical Characteristics

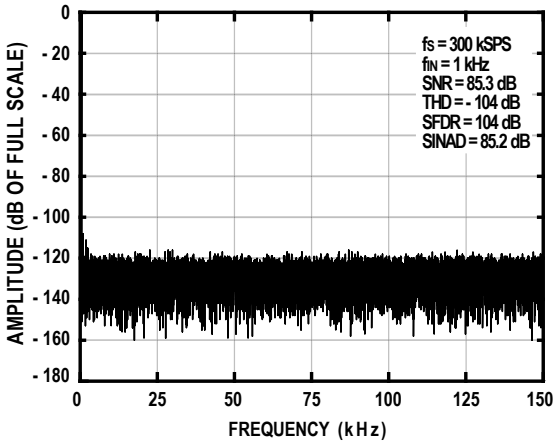

Figure 2. AC Characteristics

18/16/14-bit full speed SAR ADC ZJC2000 series is listed below:

Model	400 kSPS	500 kSPS	600 kSPS	Packages
18-bit fully differential	ZJC2000			MSOP-10 DFN-10
18-bit unipolar pseudo differential	ZJC2004			
18-bit bipolar pseudo differential	ZJC2005			
16-bit fully differential		ZJC2001		
16-bit unipolar pseudo differential		ZJC2002		
16-bit bipolar pseudo differential		ZJC2003		
14-bit unipolar pseudo differential			ZJC2007	
14-bit bipolar pseudo differential			ZJC2008	

18/16/14-bit regular speed SAR ADC ZJC2000 series are as follows:

Model	200 kSPS	250 kSPS	300 kSPS	Packages
18-bit fully differential	ZJC2010			MSOP-10 DFN-10
18-bit unipolar pseudo differential	ZJC2014			
18-bit bipolar pseudo differential	ZJC2015			
16-bit fully differential		ZJC2011		
16-bit unipolar pseudo differential		ZJC2012		
16-bit bipolar pseudo differential		ZJC2013		
14-bit unipolar pseudo differential			ZJC2017	
14-bit bipolar pseudo differential			ZJC2018	

Table of Contents

Version (Release B) [1]

Revision History

October 2023 ——Release B

English version

Format、Digital Output parameter、Figure5 updating

November 2022 ——Release A

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Pin Configurations and Function Descriptions

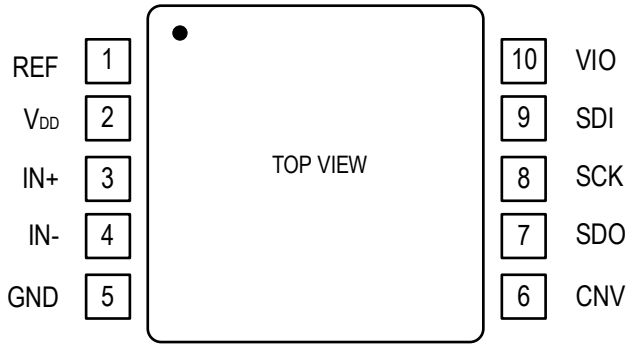


Figure 3. 10-lead MSOP Pin Configuration

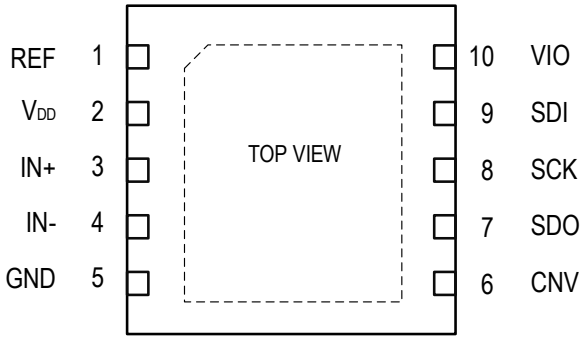


Figure 4. 10-lead DFN Pin Configuration

Note: The exposed pad has no internal connection. Connect the pad to GND.

Mnemonic	Pin No.	Pin Type	Description
REF	1	Power Supply	The voltage reference input. V_{REF} ranges from 0.5 V to V_{DD}. It is recommended that this pin must be decoupled to the GND by a 10 µF X7R ceramic capacitor as close as possible.
V_{DD}	2	Power Supply	Power Supply pin. V_{DD} ranges from 2.7 V to 5.5 V. It is recommended that V_{DD} be bypassed through a minimum of 0.1 µF ceramic capacitor to GND.
IN+	3	Analog Input	Analog input positive pin. IN+ to GND ranges from 0 V to V_{REF}. IN+ to IN- forms a pseudo differential input with an input range of 0 V to V_{REF}.
IN-	4	Analog Input	Analog input negative pin. IN- should connect to analog GND or remote GND.
GND	5	Ground	Power Ground.
CNV	6	Digital Input	Conversion input. This input has multiple functions as described in the Digital Interface section.
SDO	7	Digital Output	Serial data output. The conversion result is output through this pin. It is synchronized with SCK.
SCK	8	Digital Input	Serial data clock input. When the device is selected, the conversion result is shifted out through this clock.
SDI	9	Digital Input	Serial data input. This input provides multiple functions to implement a variety of different serial protocols.
VIO	10	Power Supply	Input/output interface digital power supply. The nominal voltage on this pin is the same as the controller interface power supply (1.8 V, 2.5 V, 3.3 V, or 5 V). It is recommended that VIO be bypassed through a minimum of 0.1 µF ceramic capacitor to GND.
EPAD			Exposed pad. Recommend connecting to ground.

Absolute Maximum Ratings [1]

Parameter	Rating
V_{DD}, REF, VIO to GND	- 0.3 V ~ 6 V
REF, VIO to V_{DD}	- 6 V ~ 0.3 V
Analog Input Range (IN+, IN− to GND)	- 0.3 V ~ V_{DD} + 0.3 V
Digital Input to GND	- 0.3 V ~ VIO + 0.3 V
Digital Output to GND	- 0.3 V ~ VIO + 0.3 V
Storage Temperature Range	- 65 °C to +150 °C
Junction Temperature Range	150 °C
Lead Temperature (Soldering, 10 seconds)	300 °C
Maximum Reflow Temperature [2]	260 °C
Electrostatic Discharge (ESD) [3]	
Human Body Model (HBM) [4]	1.5 kV
Charged Device Model (CDM) [5]	1 kV

Thermal Resistance [6]

Package Type	θ_{JA}	θ_{JC}	Unit
MSOP-10	150	50	°C/W
DFN-10	43	5.5	°C/W

[1] These ratings apply at 25 °C, unless otherwise noted. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

[2] IPC/JEDECJ–STD-020 Compliant.

[3] Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

[4] ANSI/ESDA/JEDEC JS-001 Compliant.

[5] ANSI/ESDA/JEDEC JS-002 Compliant.

[6] θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

Specifications

The ● denotes the full temperature range for specified performance. Unless otherwise noted, V_{DD} = 4.5 V ~ 5.5 V, V_{REF} = V_{DD}, T_A = 25 °C.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Resolution				14			bits
Input Characteristics							
Voltage Range		IN+ to IN-	●	0		V_{REF}	V
Absolute input voltage		IN+ to GND	●	- 0.1		V_{REF} + 0.1	V
		IN- to GND	●	- 0.1		+ 0.1	V
Common Mode Rejection Ratio	CMRR	f_{IN} = 250 kHz			57		dB
Leakage Current		Acquisition Phase			1		nA
Input Impedance [1]							
Throughput							
Conversion Rate			●			300	kSPS
Transient Response		Full - scale step	●			1.9	µs
DC Accuracy							
No Missing Codes			●	14			bits
Integral Nonlinear Error	INL		●	- 0.75	± 0.25	+ 0.75	LSB [2]
Differential Nonlinear Error	DNL		●	- 0.5	± 0.25	+ 0.5	LSB
Transition Noise		V_{REF} = V_{DD} = 5 V	●		0.3		LSB
Gain Error	GE		●	- 5	± 0.5	± 5	LSB
Gain Error Temperature Drift			●		± 0.3		ppm/°C
Zero Error	ZE		●	- 1.5	± 0.5	+ 1.5	LSB
Zero Temperature Drift					± 0.3		ppm/°C
Power Supply Sensitivity		V_{DD} = 5 V ± 5 %			± 1		ppm
AC Accuracy							
Dynamic Range	DR	V_{REF} = 5 V	●	84.5	85.5		dB [3]
SNR	SNR	f_{IN} = 1 kHz, V_{REF} = 5 V	●	83.7	85.1		dB
		f_{IN} = 1 kHz, V_{REF} = 2.5 V	●		81.5		dB

1 See the Analog Inputs section.
2 LSB means least significant bit. 1 LSB = 305.2 µV for ± 5 V input range.
3 Unless otherwise noted, all specifications expressed in decibels (dB) are referenced to full-scale input FSR and are tested with an input signal 0.5 dB below full-scale.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Spurious-Free Dynamic Range	SFDR	f_{IN} = 1 kHz, V_{REF} = 5 V			103		dB
Total Harmonic Distortion	THD				- 103		dB
Signal-to (Noise + Distortion)	SINAD	f_{IN} = 1 kHz, V_{REF} = 5 V	●	83.5	85		dB
Intermodulation Distortion	IMD	f_{IN} = 1 kHz, V_{REF} = 5 V			- 97		dB
Reference							
Voltage Range			●	0.5		V_{DD} + 0.3	V
Load Current		Sine Wave Input			100		µA
Sampling Dynamics							
- 3 dB Input Bandwidth		V_{DD} = 5 V			1.7		MHz
Aperture Delay		V_{DD} = 5 V			3		ns
Digital Input							
Logic Level	V_{IL}		●	- 0.3		0.3 x VIO	V
	V_{IH}		●	0.7 x VIO		VIO + 0.3	V
	I_{IL}		●	- 1		+ 1	µA
	I_{IH}		●	- 1		+ 1	µA
Digital Output							
Data Format				Serial 14 - bit, straight binary			
Pipeline Delay				Upon the conversion is complete, the code is ready for reading			
	V_{OL}	I_{OUT} = + 200 µA	●			0.4	V
	V_{OH}	I_{OUT} = - 200 µA	●	VIO - 0.3			V
Power Supplies							
Analog Power	V_{DD}		●	4.5		5.5	V
Digital Interface Power	VIO	Specified performance	●	2.3		V_{DD} + 0.3	V
VIO Range				1.8		V_{DD} + 0.3	V
Stand-by Current [4, 5]		V_{DD} and VIO = 5 V	●		2	50	nA
Power Consumption		V_{DD} = 5 V, 100 SPS throughput			4		µW
		V_{DD} = 5 V, 100 kSPS throughput	●		4	4.8	mW
		V_{DD} = 5 V, 300 kSPS throughput	●		9	10.5	mW
Energy per Conversion					35		nJ/sample
Temperature Range							
Specified Performance		T_{MIN} to T_{MAX}		- 40		+ 85	°C

[4] In the acquisition phase.
[5] All digital inputs are forced to VIO or GND as required.

Timing Specifications

The ● denotes the full temperature range for specified performance. Unless otherwise specified, V_{DD} = 4.5 V ~ 5.5 V, VIO = 2.3 V ~ V_{DD}, V_{REF} = V_{DD}, T_A = 25 °C.

Parameter	Symbol		Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}	●	0.4		1.4	μs
Acquisition Time	t_{ACQ}	●	1.933			μs
Time Between Conversions	t_C	●	3.333			μs
CNV Pulse Width ($\overline{CS}$ Mode)	t_{CNVH}	●	10			ns
SCK Period ($\overline{CS}$ Mode)	t_{SCK}	●	15			ns
SCK Period (Chain Mode)	t_{SCK}	●				
VIO above 4.5 V		●	17			ns
VIO above 3 V		●	18			ns
VIO above 2.3 V		●	20			ns
SCK Low Time	t_{SCKL}	●	7			ns
SCK High Time	t_{SCKH}	●	7			ns
SCK Falling Edge to Data Remain Valid	t_{HSDO}	●	4			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}					
VIO above 4.5 V		●			14	ns
VIO above 3 V		●			15	ns
VIO above 2.3 V		●			17	ns
CNV or SDI Low to SDO D15 MSB Valid ($\overline{CS}$ Mode)	t_{EN}	●				
VIO above 4.5 V		●			20	ns
VIO above 3 V		●			22	ns
VIO above 2.3 V		●			25	ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ Mode)	t_{DIS}	●			25	ns
SDI Valid Setup Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{SSDICNV}$	●	15			ns
SDI Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$	●	3			ns
SCK Valid Setup Time from CNV Rising Edge (Chain Mode)	$t_{SSCKCNV}$	●	5			ns
SCK Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSCKCNV}$	●	5			ns
SDI Valid Setup Time from SCK Falling Edge (Chain Mode)	$t_{SSDISCK}$	●	3			ns
SDI Valid Hold Time from SCK Falling Edge (Chain Mode)	$t_{HSDISCK}$	●	4			ns
SDI High to SDO High (Chain Mode with Busy Indicator)	$t_{DSDOSDI}$					
VIO above 4.5 V		●			17	ns
VIO above 2.3 V		●			27	ns

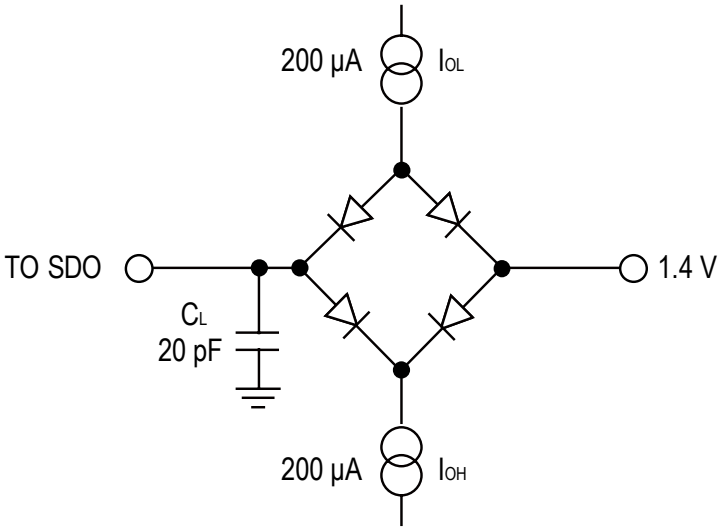


Figure 5. Load Circuit for Digital Interface Timing

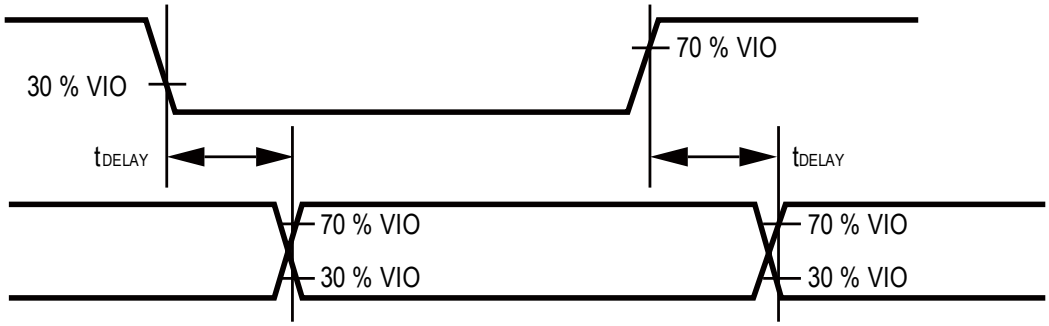


Figure 6. Voltage Levels for Timing

Typical Performance Characteristics

Unless otherwise noted, V_{DD} = 5.0 V, REF = 5.0 V, VIO = 3.3 V, T_A = 25 °C.

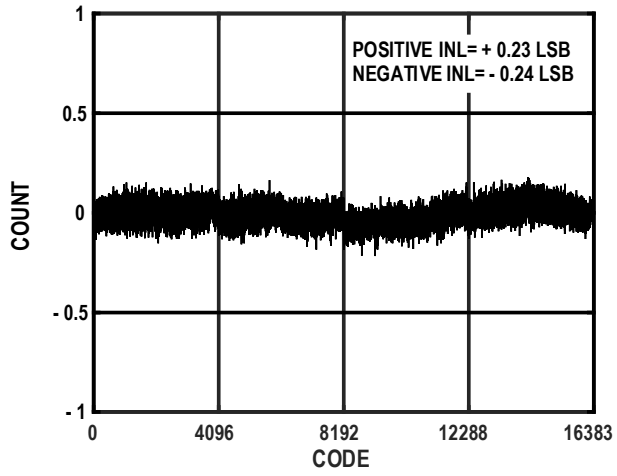


Figure 7. Integral Nonlinearity vs. Code

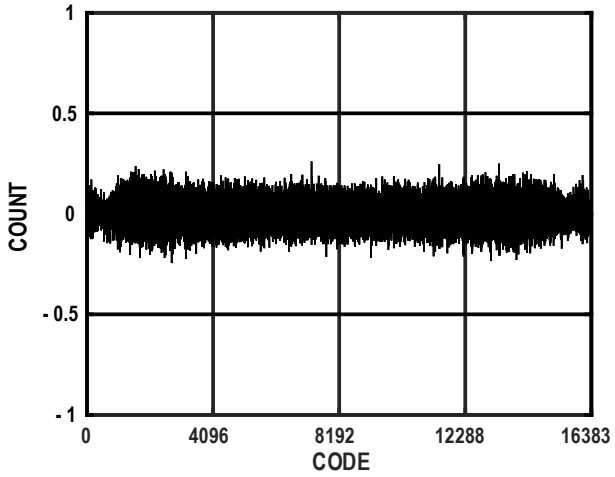


Figure 8. Differential Nonlinearity vs. Code

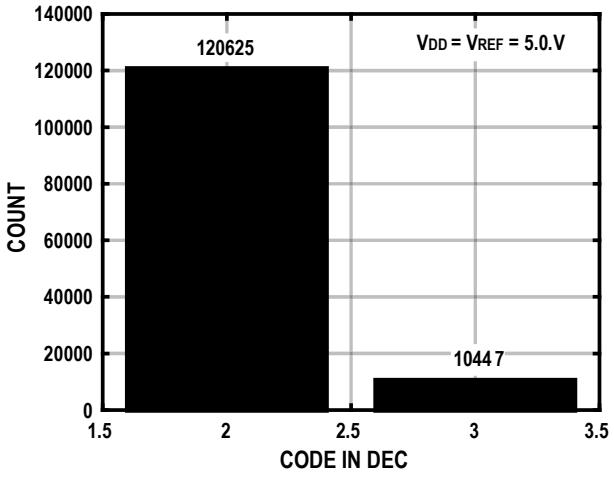


Figure 9. Histogram of DC Input (Code Center)

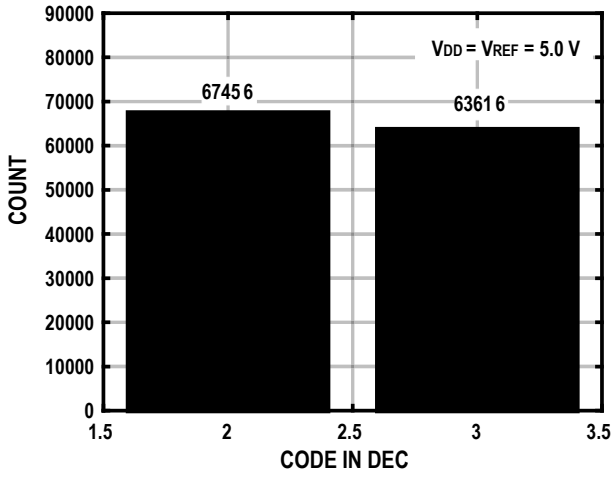


Figure 10. Histogram of DC Input (Code Transition)

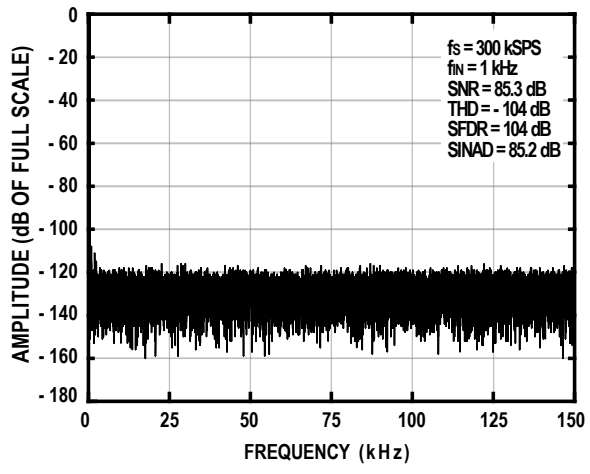


Figure 11. FFT Plot

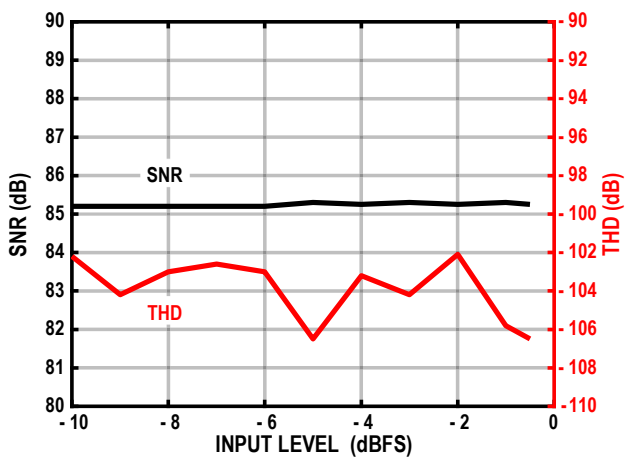


Figure 12. SNR, THD vs. Input Level

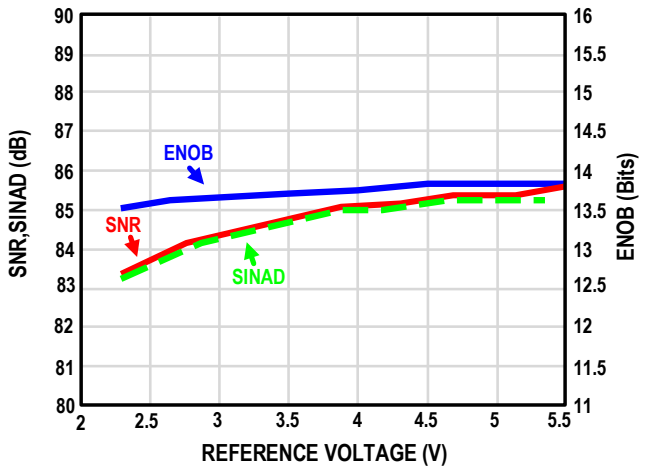


Figure 13. SINAD and ENOB vs. Reference Voltage

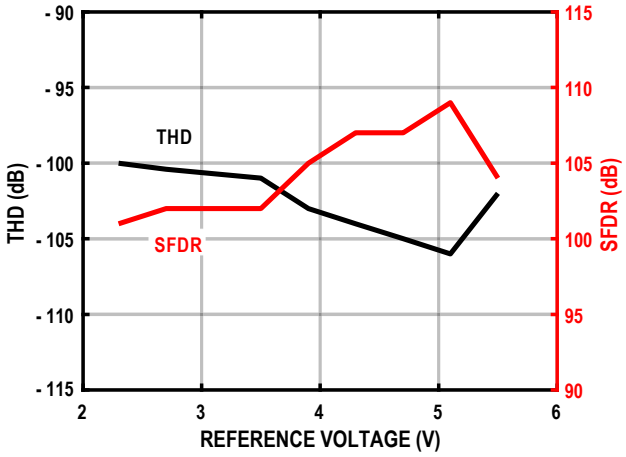


Figure 14. THD, SFDR vs. Reference Voltage

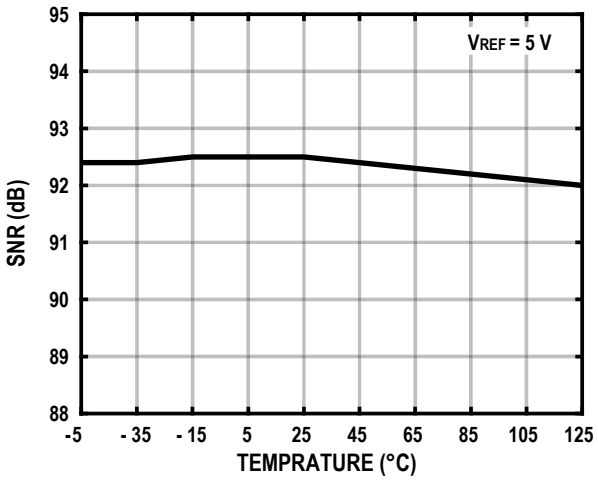


Figure 15. SNR vs. Temperature

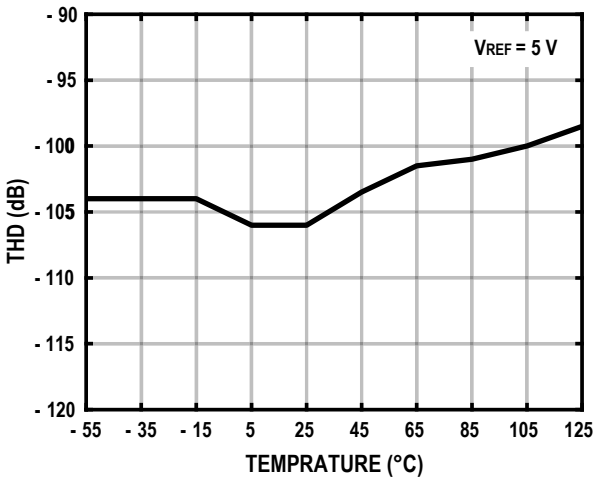


Figure 16. THD vs. Temperature

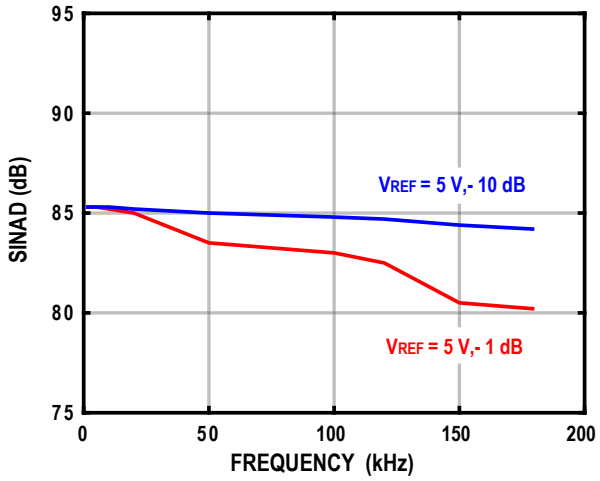


Figure 17. SINAD vs. Frequency

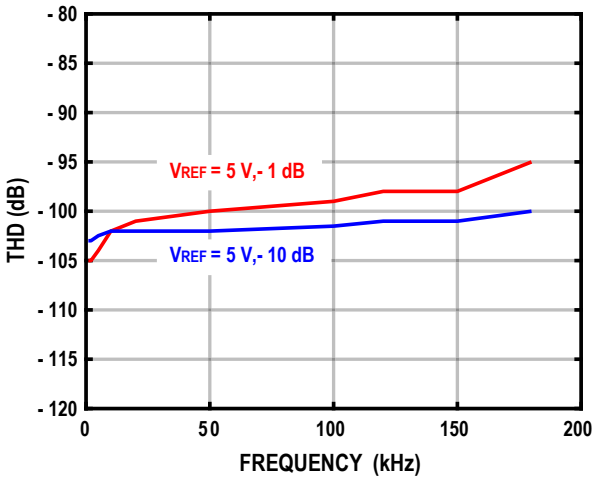


Figure 18. THD vs. Frequency

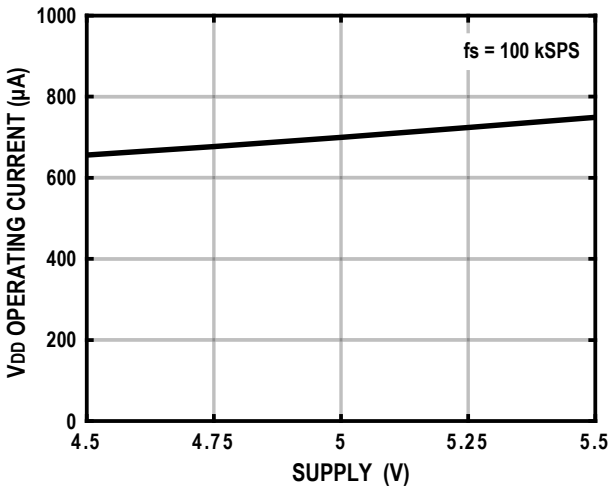


Figure 19. V_{DD} Operating Current vs. Power Supply Voltage

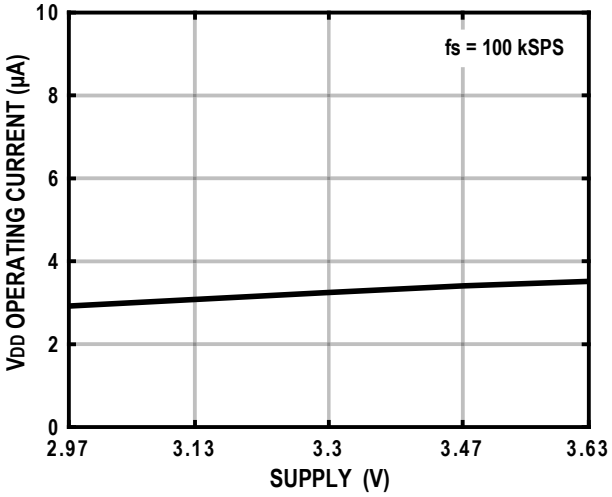


Figure 20. VIO Operating Current vs. Power Supply Voltage

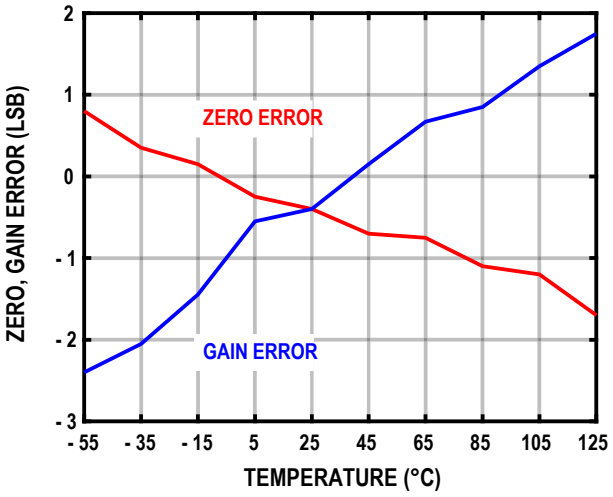


Figure 21. Zero Input, Gain Error vs. Temperature

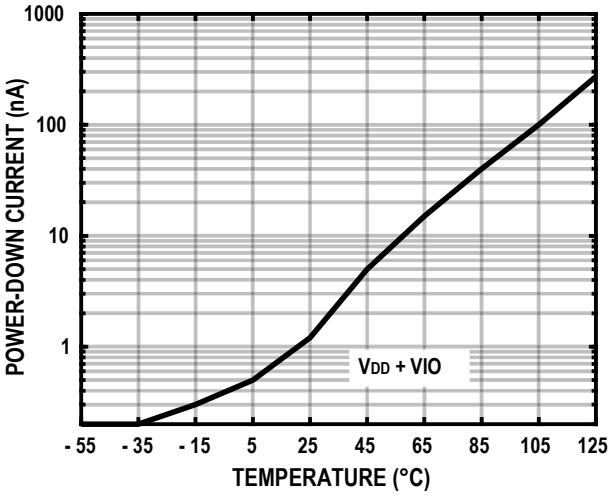


Figure 22. Stand-by Current vs. Temperature

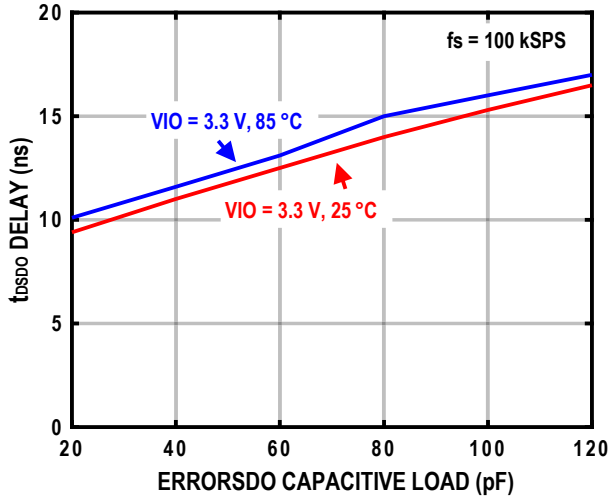


Figure 23. t_{DSDO} Delay vs Capacity Load and Voltage

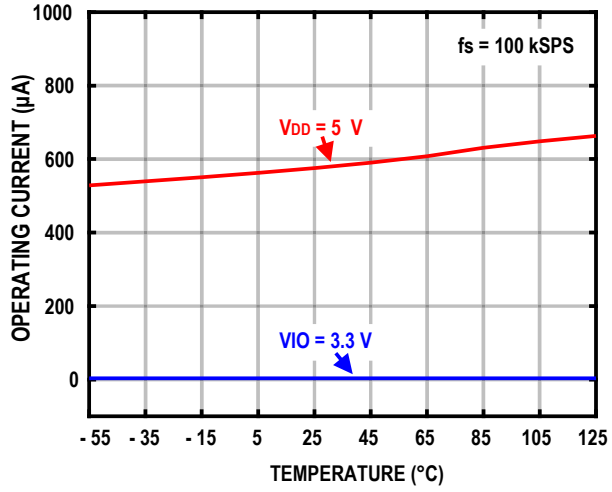


Figure 24. Operating Current vs. Temperature

Theory of Operation

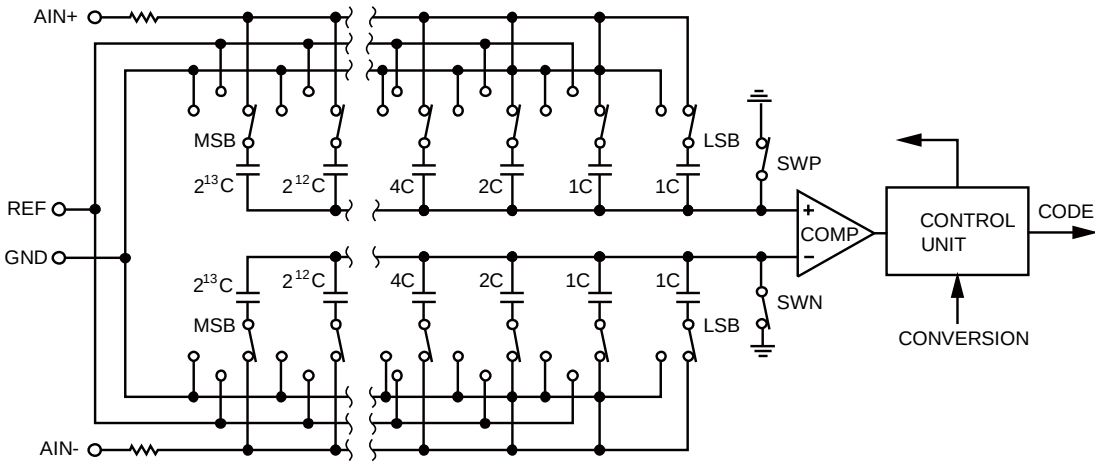


Figure 25. ADC Simplified Circuit Diagram

Circuit Structure

ZJC2017 is a fast, high precision, low power consumption, true 14-bit pseudo differential input successive approximation analog-to-digital converter (SAR ADC). The ZJC2017 is capable of converting 300 k samples per second (300 kSPS), with the device entering stand-by mode between conversions. Typical power consumption is 35 μW when operating at 1 kSPS, making it ideal for low-power applications.

The ZJC2017 can interface with any 1.8 V to 5 V (or V_{DD}) digital logic level and is available in a 10-lead MSOP package or a 10-lead DFN (LFCSP) package which saves space. It is fully pin compatible with 16-bit pseudo differential input ADC ZJC2012.

Converter Operations

Figure 25 is a simplified circuit diagram of ZJC2017. It is based on a charge redistribution DAC.

During the acquisition phase, the array node connected to the input of the comparator is short connect to GND via the SW+ and SW-. All individual switches are connected to analog inputs. Therefore, the capacitor array is used as the sampling capacitor, sampling analog signal at the IN+ and IN- input. When the acquisition phase is complete and a rising edge occurs on the CNV input, the conversion phase is initiated. When the conversion phase begins, the SW+ and SW- disconnect first. The two capacitor arrays are then disconnected from the input and connected to the GND input. By switching the elements of the capacitor array between GND and REF, the comparator input will vary in binary weighted voltage steps ($V_{REF}/2^1$, $V_{REF}/2^2$, ...,$V_{REF}/2^{13}$). The control logic toggles these switches in sequence starting with the MSB, and the comparator is brought back into balance each time. After this process is complete, the device returns to the acquisition phase, and the control logic generates the ADC output code and busy signal indication. ZJC2017 has an on-chip conversion clock, so the conversion process does not require an external serial clock SCK.

Transfer Function

The ideal transfer function of ZJC2017 is shown in Figure 26.

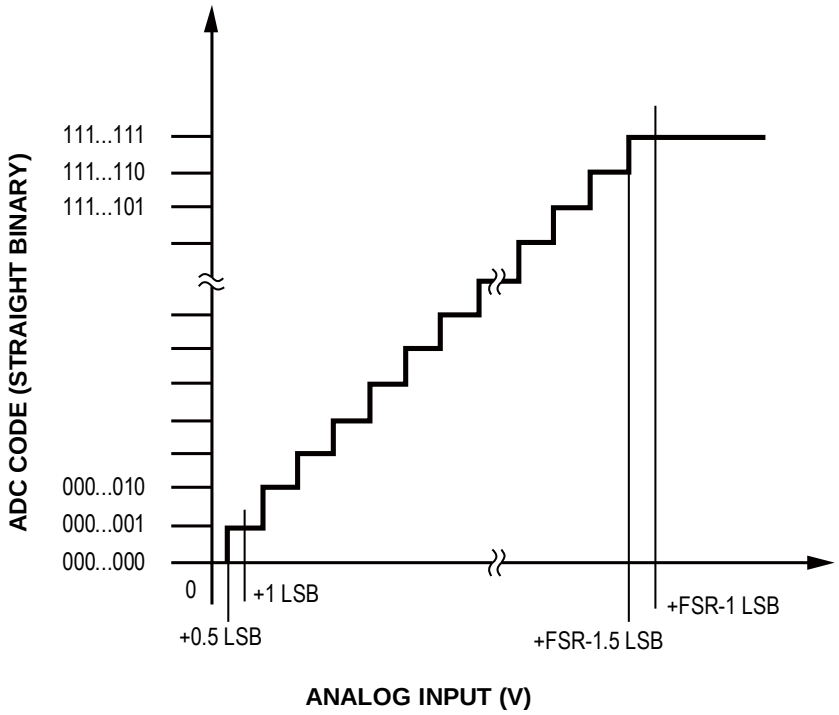


Figure 26. ADC Ideal Transfer Function

Output Code and Ideal Input Voltage:

Description	Analog Input V_{REF} = 5 V	Digital Output (Hex)
FSR - 1 LSB	+ 4.999695 V	0x3FFF [1]
Midscale + 1 LSB	2.5003052 V	0x3FFE
Midscale	2.5 V	0x2000
Midscale - 1 LSB	2.499695 V	0x1FFF
- FSR + 1 LSB	305.2 µV	0x0001
- FSR	0 V	0x0000 [2]

[1] 这也是超量程模拟输入 (VIN+ – VIN–高于 V_{REF} – V_{GND}) 对应的代码。
[2] 这也是欠量程模拟输入 (VIN+ – VIN–低于 V_{GND}) 对应的代码。

Typical Connection Diagram

Figure 27 is a suggested connection diagram for the ZJC2017 when multiple power supplies are used.

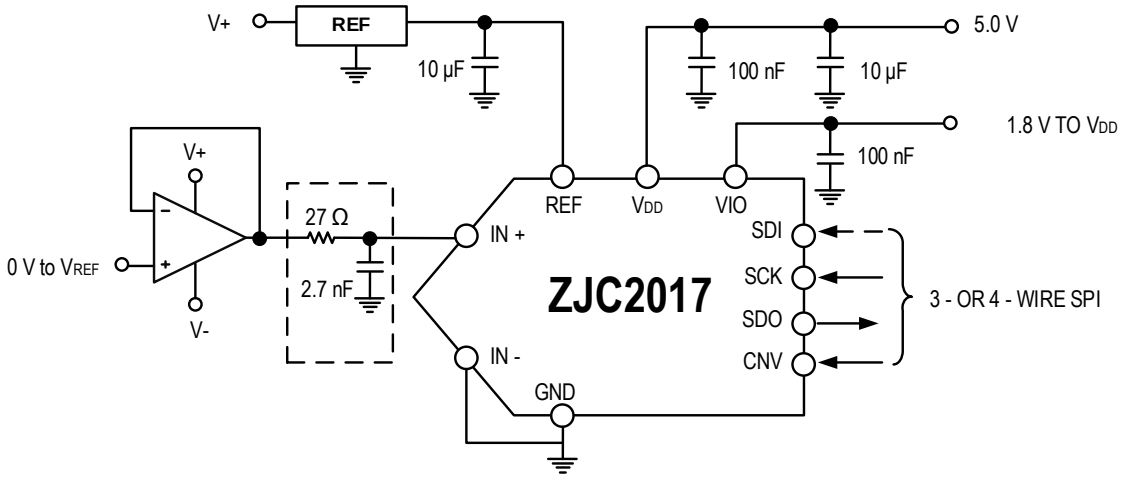


Figure 27. Application Circuits Using Multiple Power Supplies

Figure 28 shows the equivalent circuit of the ZJC2017 input structure.

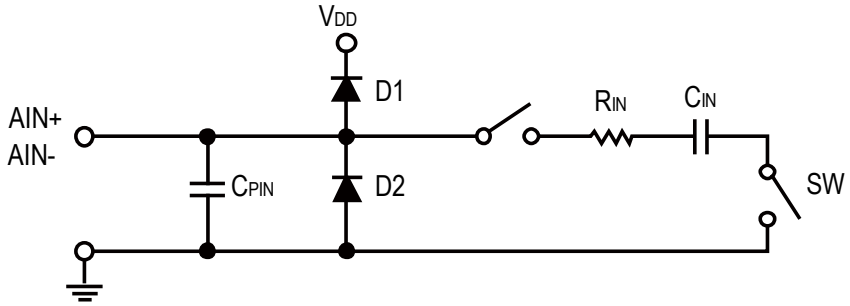


Figure 28. Two Diodes D1 and D2 Provide ESD Protection for the Analog Inputs

Note that the voltage of the analog input signal cannot be higher than the supply voltage (V_{DD}) by more than 0.3 V. If the voltage of the analog input signal exceeds V_{DD} + 0.3 V, the diode will be forward biased and start conducting current. These two diodes can handle forward bias currents up to 50 mA. If the supply voltage of the input driver is higher than V_{DD} the voltage of the analog input signal may be more than 0.3 V higher than the supply voltage. The two diodes D1 and D2 provide ESD protection for analog input IN+ and IN-.

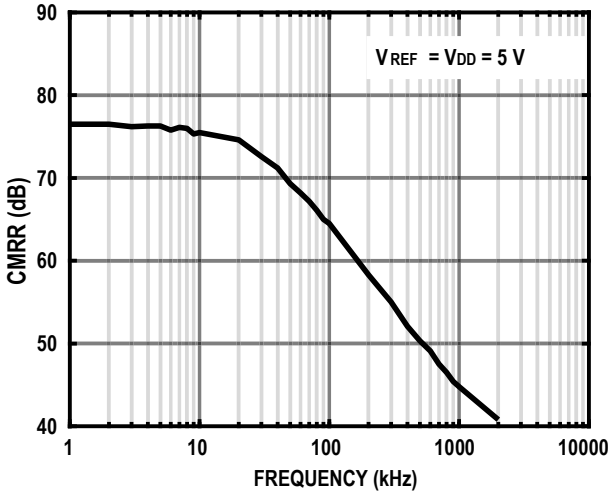


Figure 29. Analog Input CMRR vs. Frequency

During the acquisition phase, the impedance of the analog input (IN+) can be seen as the parallel combination of the network formed by R_{IN} and C_{IN} in series and the capacitor C_{PIN}. C_{PIN} mainly includes pin capacitance. R_{IN} typical value is 4 kΩ and is a lumped element consisting of the series resistance and the on-resistance of the switch. C_{IN} typical value is 30 pF and consists mainly of the ADC sampling capacitor. High source impedance can significantly affect AC characteristics, especially harmonic distortion. THD degradation is a function of source impedance and analog input frequency.

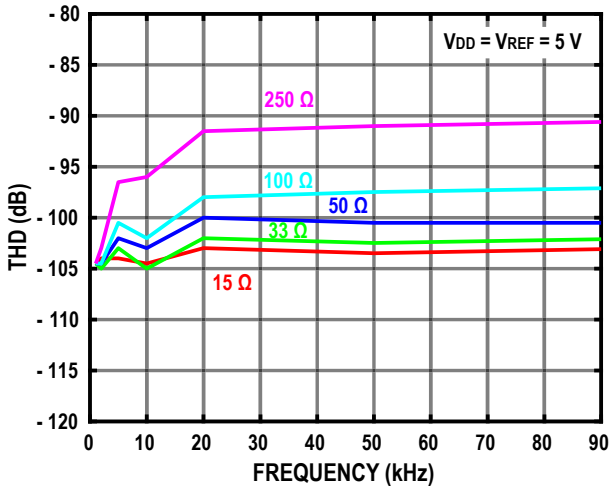


Figure 30. THD vs. Analog Input Frequency and Source Resistance

Fully Differential to Single-ended Driver

For applications using fully differential analog signals (bipolar or unipolar), an op amp driver can provide pseudo differential unipolar input to the ZJC2017, see Figure 31 for the schematic diagram.

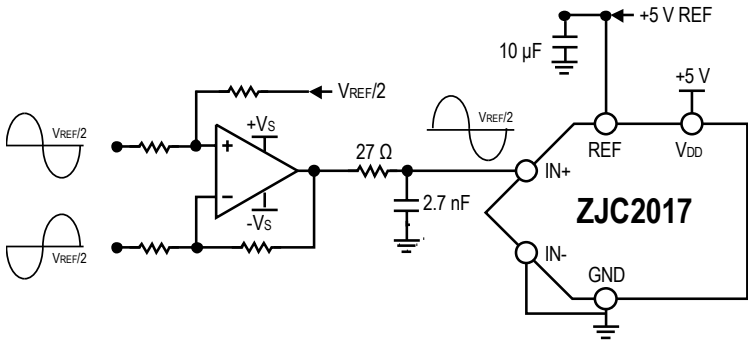


Figure 31. Fully Differential to Single-ended Conversion with an Op Amp

Singled-ended bipolar signal can be converted to pseudo differential unipolar signal with two amplifiers for ZJC2017.

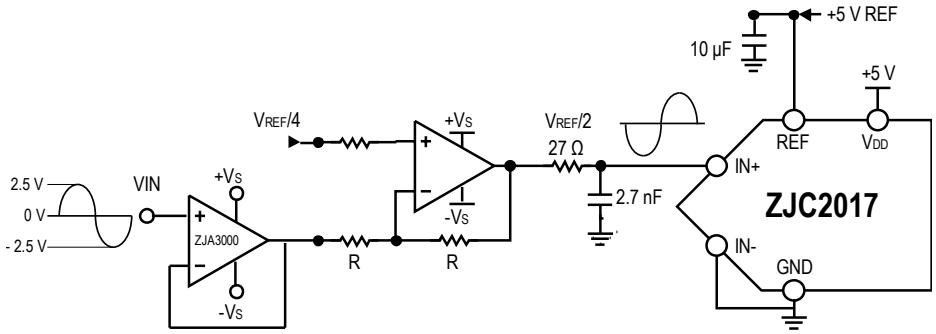


Figure 32. Single-ended Bipolar to Pseudo Differential Unipolar

Reference Voltage Input

For high-precision ADC applications, a precision voltage reference is an essential device. Generally, for 14-bit ADCs, the reference source needs to have low initial error, low noise, and low temperature drift. The ZJC2017 reference voltage REF has a dynamic input impedance, so it should be driven with a low impedance source. The REF and GND pins should be effectively decoupled as described in the PCB Layout Guidelines section. Figure 33 shows an example of a specific voltage reference and driver design. The ZJR100X series of high-precision voltage references can just meet these requirements.

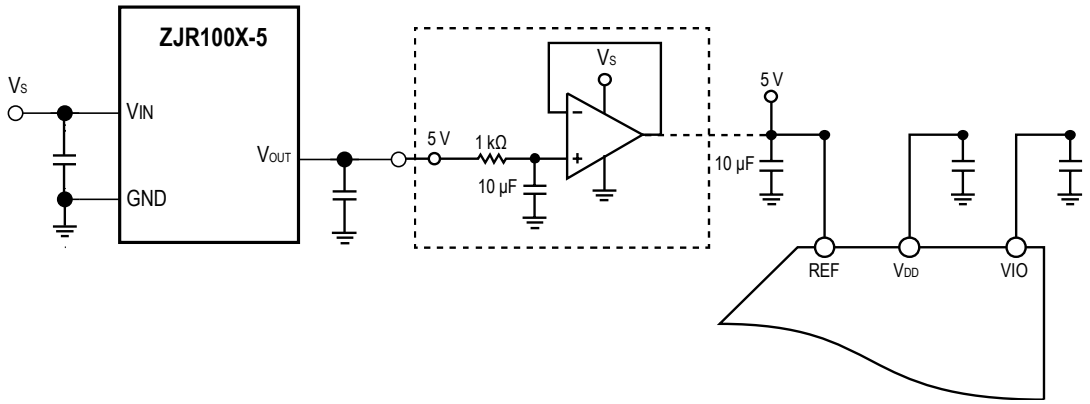


Figure 33. ZJC2017 Reference Pin Drive

Power Supply

ZJC2017 uses two power supply pins: core power supply (V_{DD}) and digital input/output interface power supply VIO. VIO can directly

interface with any logic from 1.8 V to V_{DD}. To reduce the number of power supplies required, the VIO and V_{DD} pins can be tied together via resistors or ferrite beads. The PSRR curve is shown in Figure 34.

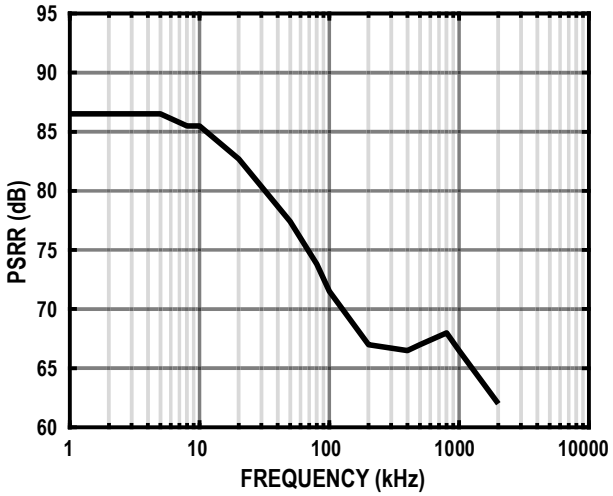


Figure 34. PSRR vs. Frequency

The ZJC2017 automatically enters stand-by mode at the end of each conversion stage, so the power consumption is approximately linearly proportional to the sampling rate. This makes the device suitable for low sampling rate and low power consumption applications. As shown Figure 35.

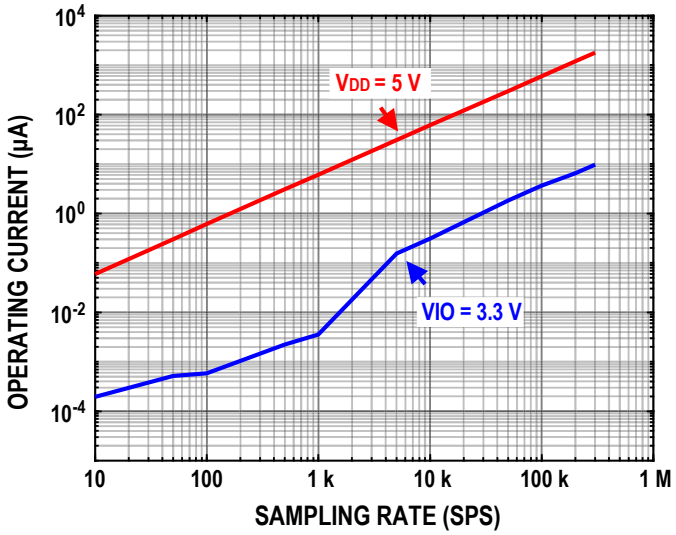


Figure 35. Operating Current vs. Sampling Rate

Digital Interface

ZJC2017 has great flexibility in serial interface mode. In $\overline{CS}$ mode, ZJC2017 is compatible with SPI, MCU and DSP. In this mode, ZJC2017 can use 3-wire or 4-wire interface. The 3-wire interface uses CNV, SCK, and SDO signals. The 4-wire interface uses the SDI, CNV, SCK, and SDO signals, with CNV for initiating conversions independent of the read back timing (SDI). In the chain mode, ZJC2017 provides the daisy chain feature, which allows the cascading of multiple ADCs. If SDI is high, $\overline{CS}$ mode is selected, and if SDI is low, chain mode is selected. Chain mode is always selected when SDI and CNV are connected together.

ZJC2017 can provide the option to forcibly add a start bit before the data bits. This start bit can be used as a busy indication. If there is no busy indication, the controller must wait for the maximum conversion time before reading back the code value. The busy indication function is enabled under the following conditions:

- In $\overline{CS}$ mode, CNV or SDI is low at the end of ADC conversion (see Figure 39 and Figure 43).
- In chain mode, SCK is high during the rising edge of CNV (see Figure 47).

$\overline{CS}$ Mode (3-Wire without Busy Indication)

This mode can be used when a single chip ZJC2017 is connected to an SPI compatible controller. The connections are shown in Figure 36 and the corresponding timing is shown in Figure 37.

While SDI is high, a rising edge on CNV initiates a conversion, selects chip-select mode, and forces SDO into a high-impedance state. Once a transition is initiated, the transition will execute to completion regardless of the state of CNV. CNV must return high before the minimum conversion time elapses and then remain high for the maximum possible conversion time to avoid generating a busy signal indication. After the conversion is completed, the ZJC2017 enters the acquisition phase and enters the stand-by mode.

When CNV goes low, the MSB is output on SDO. The remaining data bits are clocked out on subsequent falling edges of SCK. After the 14th SCK falling edge, or when CNV goes high, whichever occurs first, SDO returns to a high-impedance state.

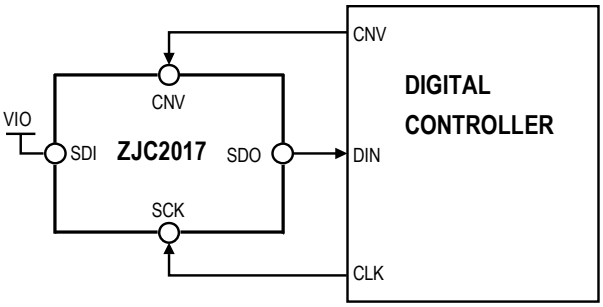


Figure 36. $\overline{CS}$ Mode (3-wire without Busy Indication) Connection Diagram

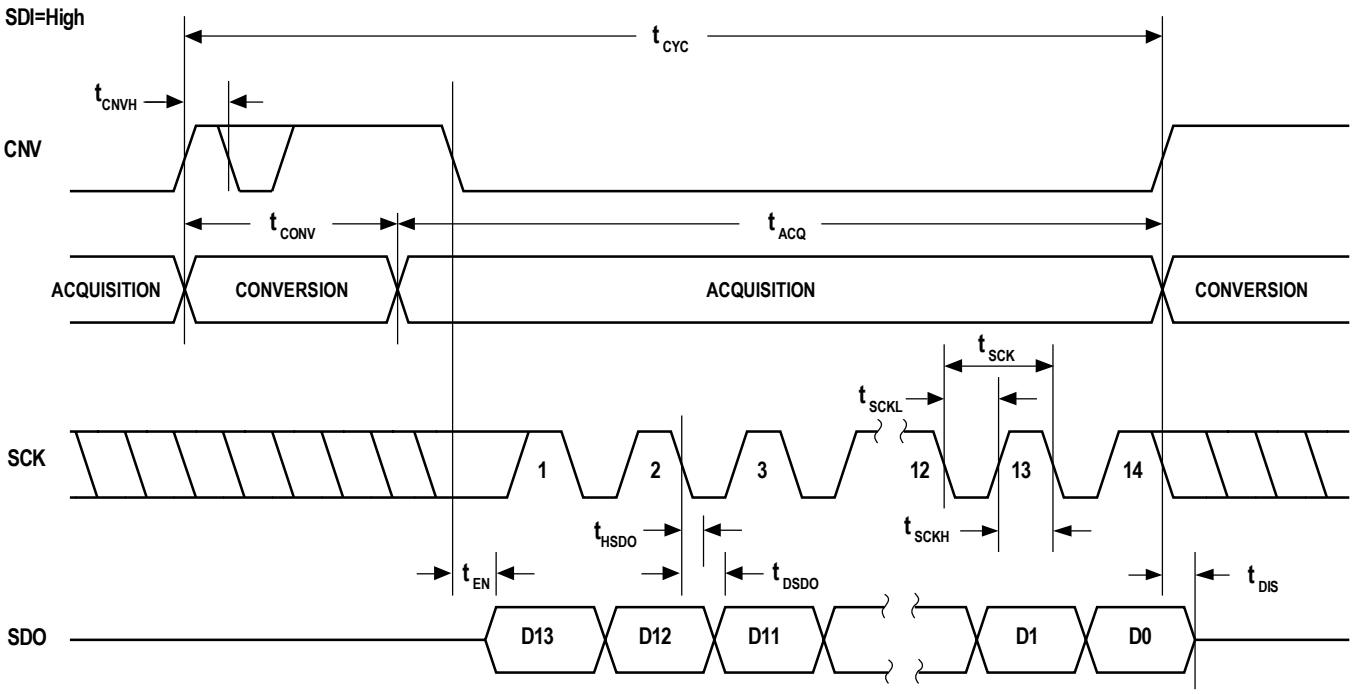


Figure 37. $\overline{CS}$ Mode (3-Wire without Busy Indication) Serial Interface Timing

$\overline{CS}$ Mode (3-Wire with Busy Indication)

This mode can be used when a single ZJC2017 is connected to an SPI-compatible digital host with an interrupt input. The connections are shown in Figure 38 and the corresponding timing is shown in Figure 39.

When connecting SDI to VIO, a rising edge on CNV initiates a conversion, selects $\overline{CS}$ mode, and forces SDO into a high-impedance state. Regardless of the state of CNV, SDO remains high impedance until the conversion is complete. CNV must return to low before the minimum transition time has elapsed and then remain low for the maximum possible transition time to guarantee a busy signal indication. When the transition is complete, SDO changes from a high-impedance state to a low-impedance state. Combined with a pull-up resistor on the SDO line, this transition can be used as an interrupt signal. Next ZJC2017 enters the acquisition stage and enters the stand-by mode. Data bits are clocked out on subsequent falling edges of SCK, MSB first. After the optional 15th SCK falling edge, or when CNV goes high, whichever occurs first, SDO returns to a high-impedance state.

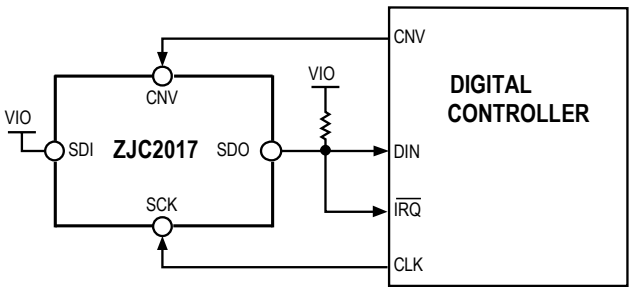


Figure 38. Chip Select Mode (three-wire type with busy indication) Connection Diagram

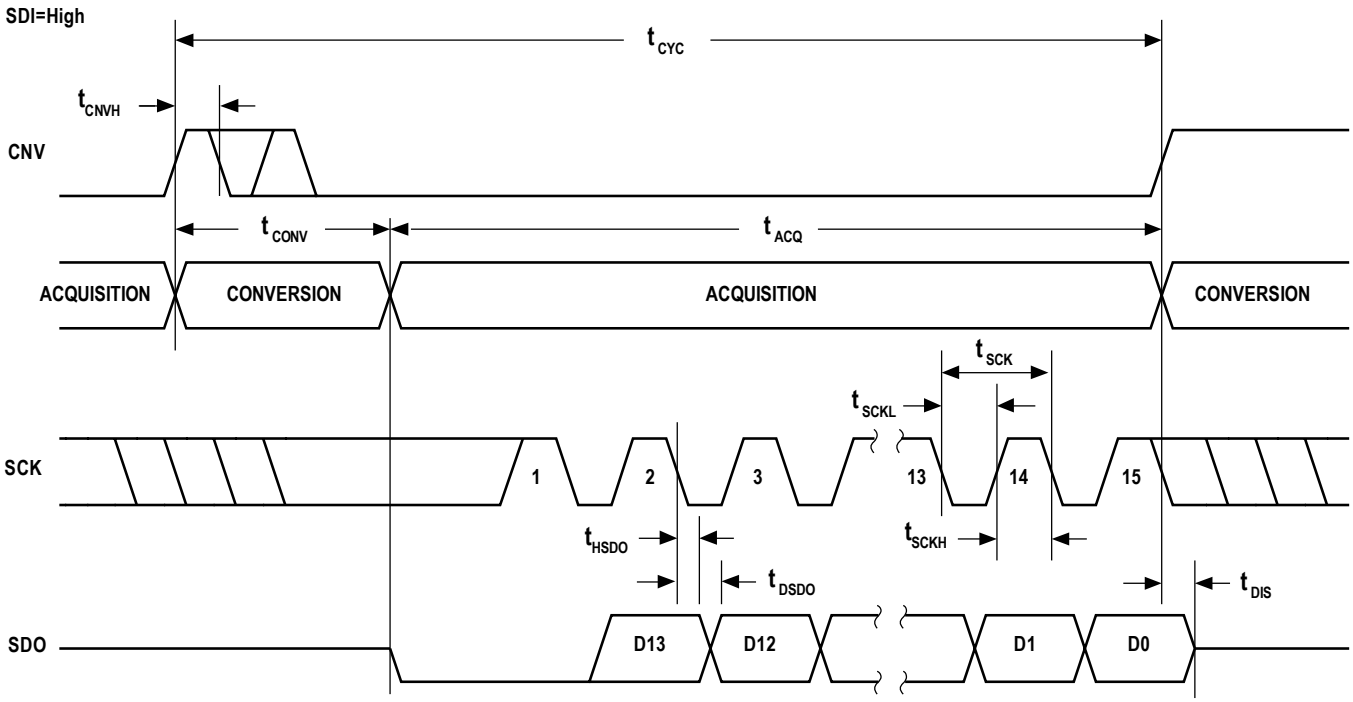


Figure 39. $\overline{CS}$ Mode (3-Wire with Busy Indication) Serial Interface Timing

$\overline{CS}$ Mode (4-wire without Busy Indication)

An example using two ZJC2017s is shown in Figure 40, and the corresponding timing is shown in Figure 41.

With SDI high, a rising edge on CNV initiates a conversion, selects $\overline{CS}$ mode, and forces SDO into a high-impedance state. In this mode, CNV must be held high during the conversion phase and subsequent data readback. If SDI and CNV are low, SDO goes low.

SDI must keep or return high before the minimum transition time elapses and then remain high for the maximum possible transition time to avoid generating a busy signal indication. After the conversion is completed, the ZJC2017 enters the acquisition phase and enters the stand-by mode. Each ADC converted code value can be read by pulling the SDI input low, which outputs the MSB to SDO. The remaining data bits are clocked out on subsequent SCK falling edges. After the 14th SCK falling edge, or when SDI goes high, whichever occurs first, SDO returns to high impedance and another ZJC2017 can be read.

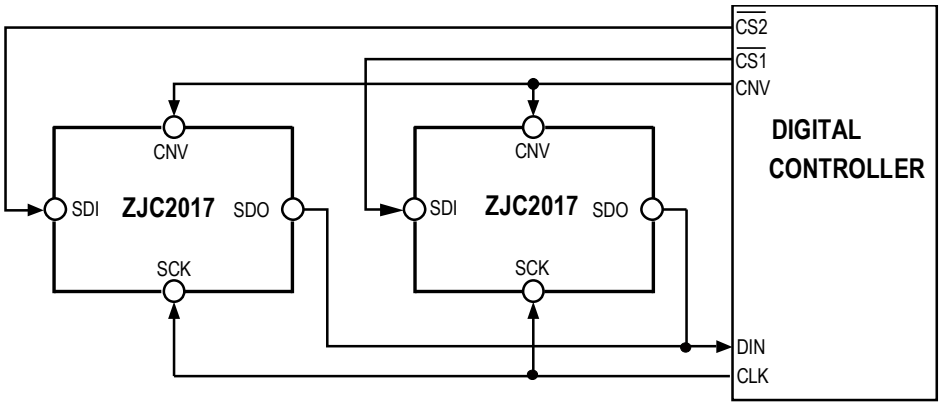


Figure 40. $\overline{CS}$ Mode (4-wire without Busy Indication) Connection Diagram

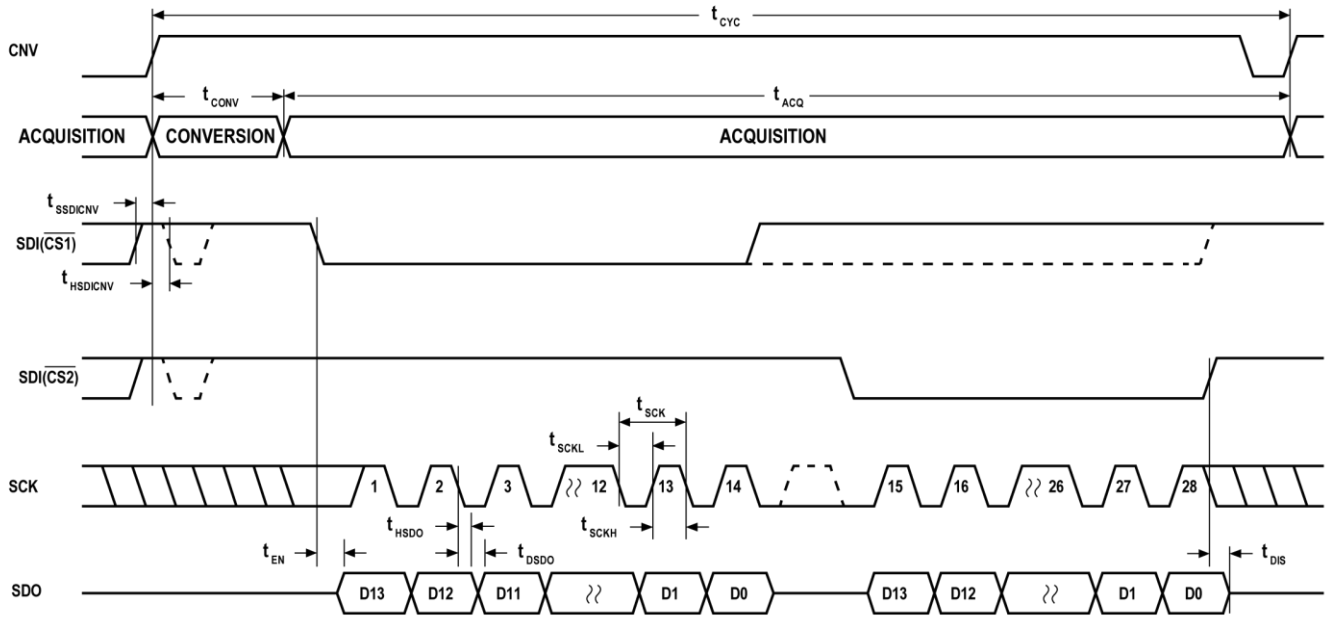


Figure 41. $\overline{CS}$ Mode (4-Wire without Busy Indication) Serial Interface Timing

$\overline{CS}$ Mode (4-Wire with Busy Indication)

The connection is shown in Figure 42 and the corresponding timing is shown in Figure 43.

With SDI high, a rising edge on CNV initiates a conversion, selects $\overline{CS}$ mode, and forces SDO into a high-impedance state. In this mode, CNV must be held high during the conversion phase and subsequent data readback. If SDI and CNV are low, SDO goes low. SDI must return low before the minimum transition time elapses and then remain low for the maximum possible transition time to guarantee a busy signal indication. When the transition is complete, SDO changes from a high-impedance state to a low-impedance state. Combined with a pull-up resistor on the SDO line, this transition can be used as an interrupt signal to initiate data readback. Next, ZJC2017 enters the acquisition phase and is on stand-by. Data bits are clocked out on subsequent falling edges of SCK, MSB first. After the optional 15th SCK falling edge or after SDI goes high, whichever occurs first, SDO returns to a high-impedance state.

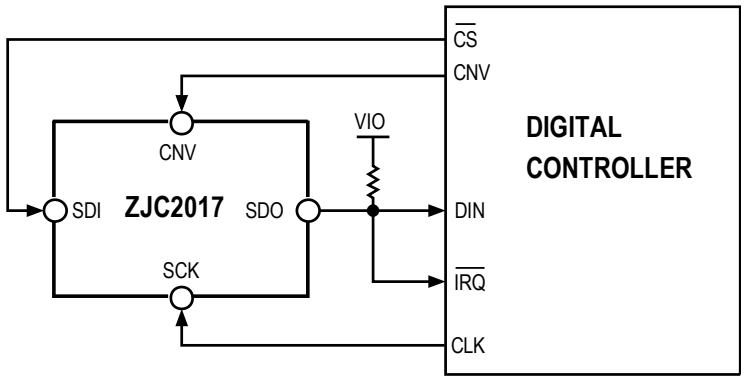


Figure 42. $\overline{CS}$ Mode (4-Wire with Busy Indication) Connection Diagram

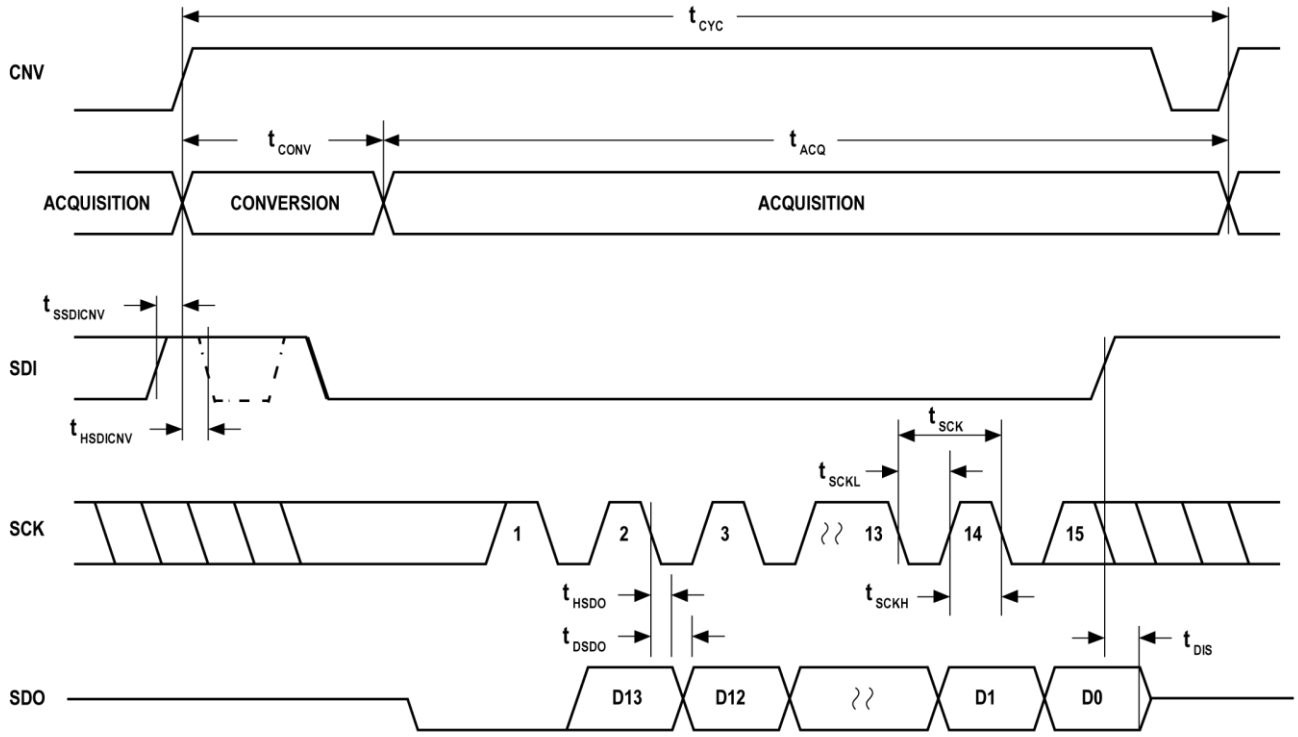


Figure 43. $\overline{CS}$ Mode (4-wire with Busy Indication) Serial Interface Timing

Chain Mode (without Busy Indication)

This mode can be used to daisy-chain multiple ZJC2017s over a three-wire serial interface.

An example using two ZJC2017s is shown in Figure 44, and the corresponding timing is shown in Figure 45.

When SDI and CNV are low, SDO goes low. With SCK low, a rising edge on CNV initiates a conversion, selects chain mode, and disables the busy indication. In this mode, CNV remains high during the conversion phase and subsequent data readback. After the conversion is completed, the MSB is output to SDO, and ZJC2017 enters the acquisition phase and stands by. The remaining data bits stored in the internal shift register are clocked out on subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked out by SCK falling edge. Each ADC in the chain outputs the data MSB first, and it takes 14×N clocks to read back N ADCs.

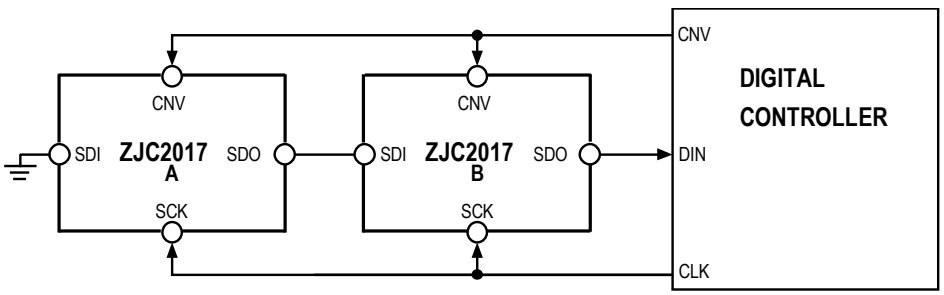


Figure 44. Chain Mode (without Busy Indication) Connection Diagram

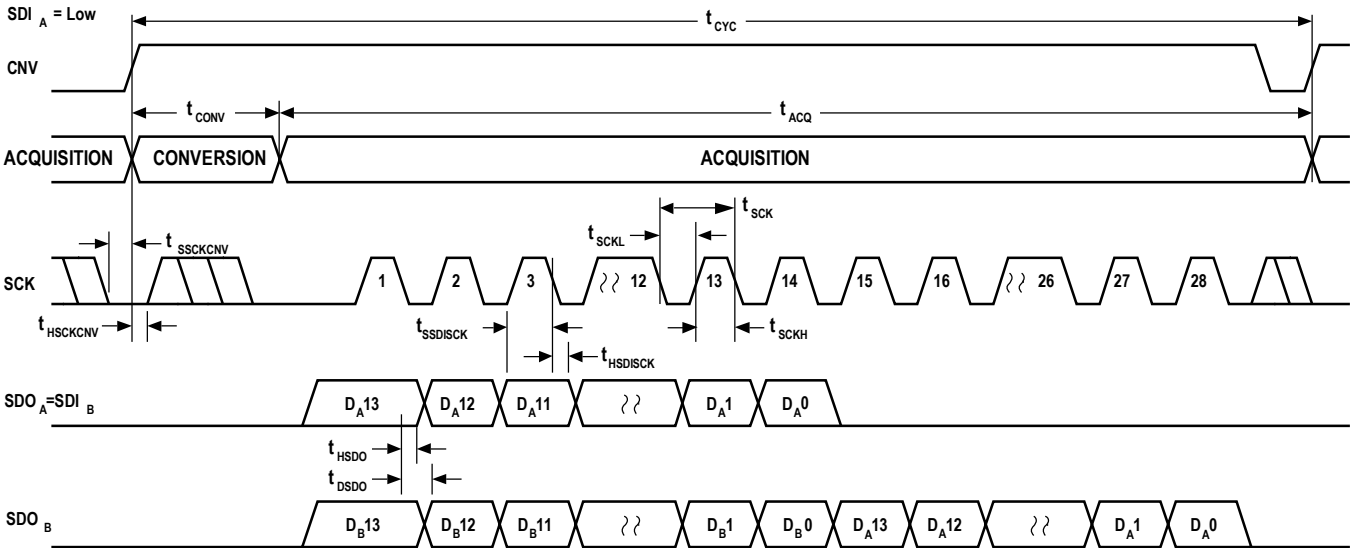


Figure 45. Chain Mode (without Busy Indication) Serial Interface Timing

Chain Mode (with Busy Indication)

This mode can also be used to daisy-chain multiple ZJC2017s on the 3-wire serial interface while providing a busy indication.

An example using three ZJC2017s is shown in Figure 46, and the corresponding timing is shown in Figure 47.

When SDI and CNV are low, SDO goes low. With SCK high, a rising edge on CNV initiates a conversion, selects chain mode, and enables the busy indicator feature. In this mode, CNV remains high during the conversion phase and subsequent data readback. After all the ADCs in the chain have completed their conversions, drive the SDO pin of the ADC closest to the digital host (see Figure 46 This transition on SDO can be used as a busy indicator to trigger data readback. ZJC2017 then enters the acquisition phase and is on stand-by. The remaining data bits stored in the internal shift register are clocked out MSB first on subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked out by SCK falling edge. Each ADC in the chain outputs data MSB first, and 14×N + 1 clocks are required to read back N ADCs.

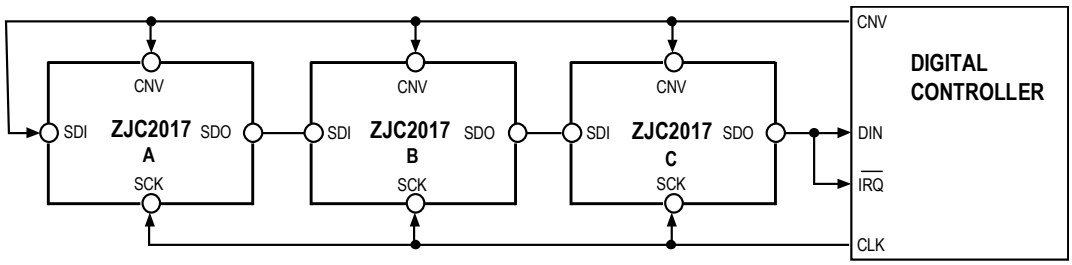


Figure 46. Chain Mode (with Busy Indication) Connection Diagram

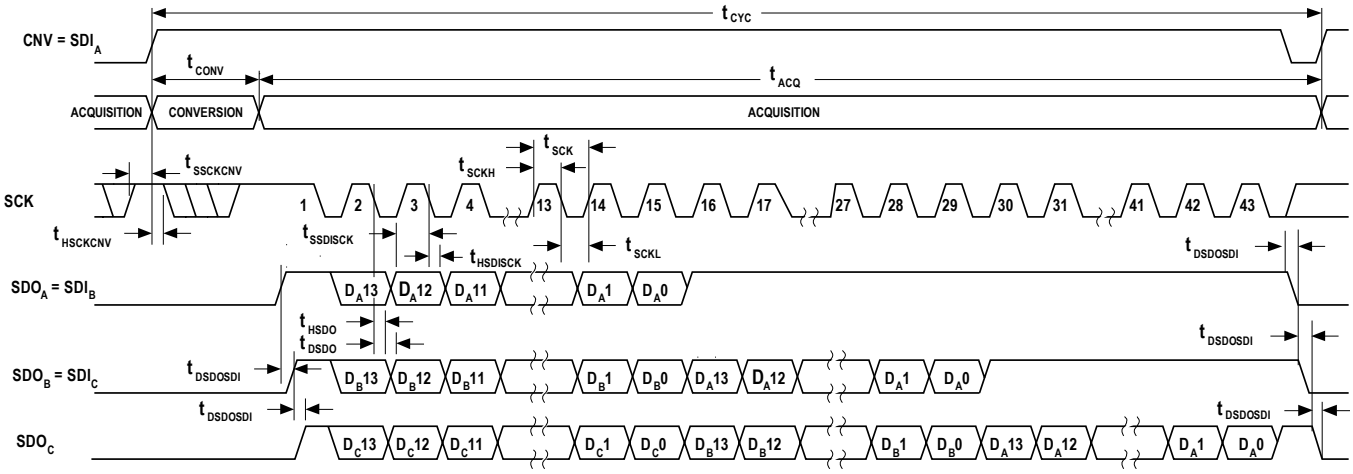


Figure 47. Chain Mode (with Busy Indication) Serial Interface Timing

Layout Guidelines

For optimum performance of the device, good PCB layout practices are recommended, including:

- It is recommended that to use a design that separates the analog part and the digital part on the ZJC2017 PCB, and each is limited to a certain area of the circuit board.
- Avoid running digital lines under the device, which may couple noise onto the die, unless a ground plane under the ZJC2017 is used as a shield. Fast switching signals such as CNV or clocks should not be placed close to the analog signal path. Crossover of digital and analog signals should be avoided.
- At least one ground plane should be used. It can be common or split between the digital and analog sections. In the latter case, the planes should be joined close to the ZJC2017.
- The ZJC2017 voltage reference input, REF, has a dynamic input impedance and should be decoupled with 10 µF ceramic capacitors to minimize parasitic inductances. This is done by placing the reference decoupling ceramic capacitor close to, ideally right up against, the REF and GND pins and connecting them with wide, low impedance trace
- The power supply V_{DD} of ZJC2017 should be decoupled with 10 µF and 100 nF ceramic capacitors, placed close to the ZJC2017 and connected using short, wide traces to provide low impedance paths and to reduce the effect of noises on the power supply lines.

Figure 48 is an example of the guidance.

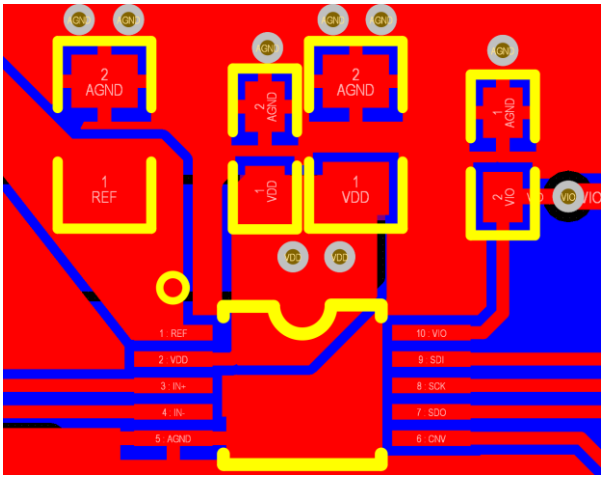


Figure 48. Example Layout and Routing of ZJC2017

Outline Dimensions

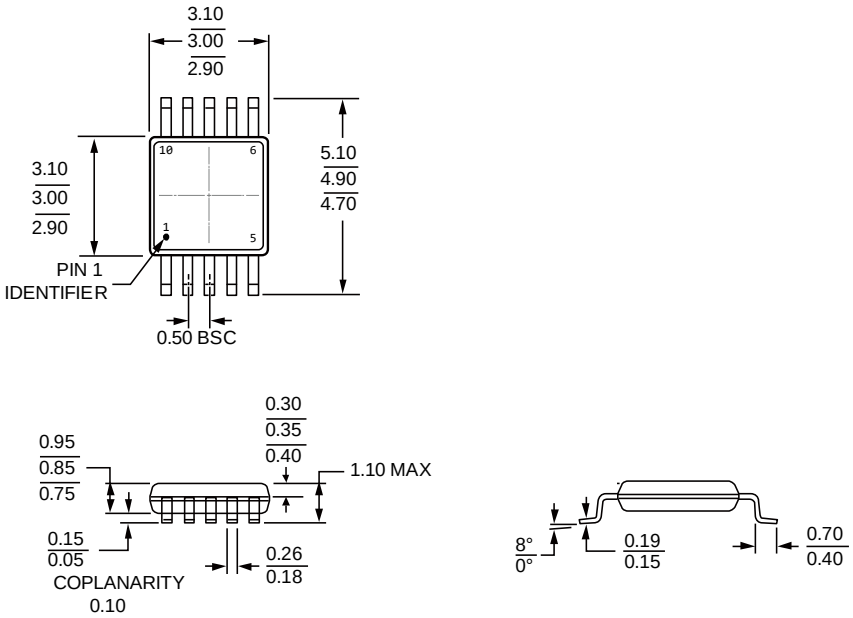


Figure 49. 10-Lead MSOP Package Dimensions Shown in Millimeter

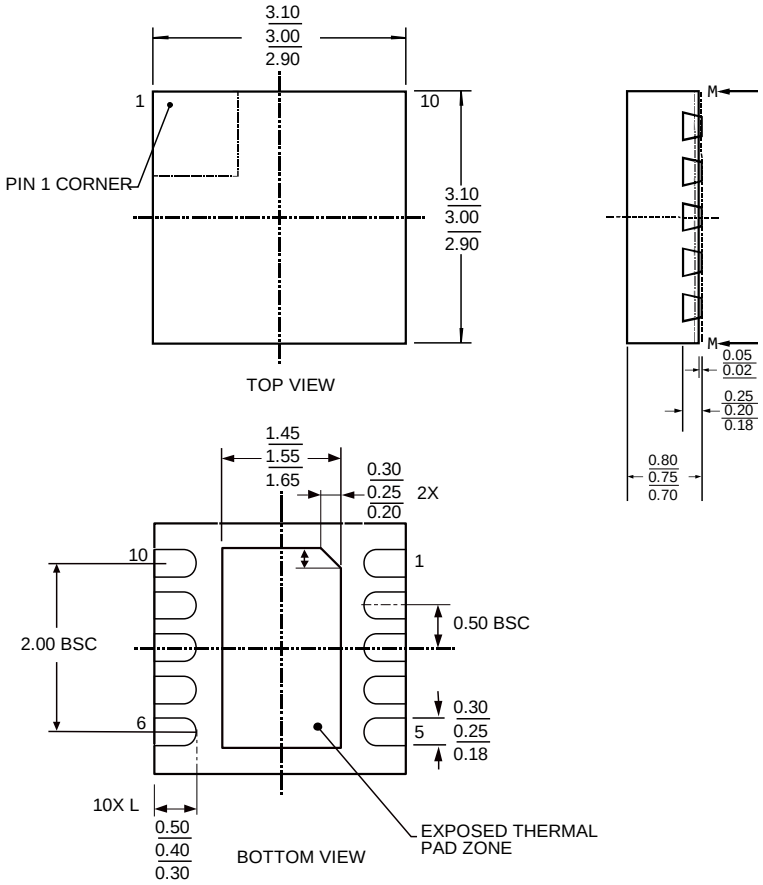
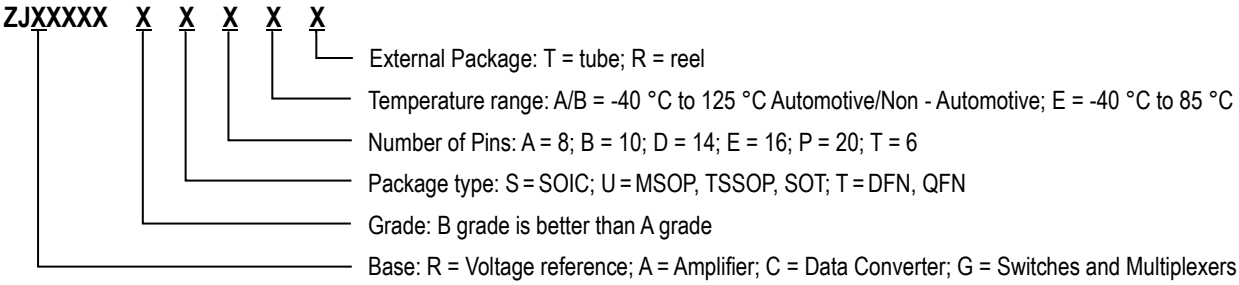


Figure 50. 10-Lead DFN Package Dimensions Shown in Millimeter

Ordering Guide

Model	Package	Orderable Device	Resolution (bit)	Supply Voltage (V)	Temperature Range (°C)	External Package
ZJC2017	MSOP-10	ZJC2017AUBET	14	4.5 to 5.5	- 40 to +85	Tube
	MSOP-10	ZJC2017AUBER				13” Reel
	DFN-10	ZJC2017ATBER				13” Reel

Product Order Model



Related Parts

PART NUMBER	DESCRIPTION	COMMENTS
ADC		
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD - 113 dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD - 113 dB
ZJC2002/2012 ZJC2003/2013	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91.7 dB, THD - 105 dB Pseudo-differential bipolar input, SINAD 91.7 dB, THD - 105 dB
ZJC2004/2014 ZJC2005/2015	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD - 105 dB Pseudo-differential bipolar input, SINAD 94.2 dB, THD - 105 dB
ZJC2007/2017 ZJC2008/2018	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD - 105 dB Pseudo-differential bipolar input, SINAD 85 dB, THD - 105 dB
ZJC2100/1-18	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD - 113 dB	
ZJC2100/1-16	16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD - 113 dB	
ZJC2102/3-18	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD - 105 dB	
ZJC2102/3-16	16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD - 105 dB	
ZJC2102/3-14	14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD - 105 dB	
ZJC2104/5-18	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD - 105 dB	
ZJC2104/5-16	16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD - 105 dB	
DAC		
ZJC2541-18/16/14 ZJC2543-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or V_{REF}/2 (ZJC2543), 1 nV-S glitch, SOIC-8/MSOP-10/DFN-10 packages
ZJC2542-18/16/14 ZJC2544-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or V_{REF}/2 (ZJC2544), 1 nV-S glitch, SOIC-14/TSSOP-16/QFN-16 packages
Amplifier		
ZJA3000-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz GBW, 35 µV max Vos, 0.5 µV/°C max Vos drift, 25 pA max Ibias, 1 mA/Amplifier, input to V-, RRO, 4.5 V to 36 V
ZJA3001-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz GBW, 35 µV max Vos, 0.5 µV/°C max Vos drift, 25 pA max Ibias, 1 mA/Amplifier, RRO, 4.5 V to 36 V
ZJA3512-2/4	Dual/Quad 36 V 7 MHz precision JFET Op Amps	7 MHz GBW, 35 V/µS SR, 50 µV max Vos, 1 µV/°C max Vos drift, 2 mA/Amplifier, RRO, 4.5V to 35 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G = 1), 25 pA max Ibias, 25 µV max Vosi, gain error 0.001 % max (G = 1), 625 kHz BW (G = 10), 3.3 mA/Amplifier, ± 2.4 V to ± 18 V, - 40 °C to 125 °C specified
ZJA3622/8	36 V low cost precision in-amp	CMRR 93 dB min (G = 10), 0.5 nA max Ibias, 125 µV max Vosi, 625 kHz BW (G = 10), 3.3 mA/Amplifier, ± 2.4 V to ± 18 V
ZJA3611, ZJA3609	36 V ultra-high precision wider bandwidth precision in-amp (min gain of 10)	CMRR 120 dB min (G = 10), 25 pA max Ibias, 25 µV max Vosi, 1.2 MHz BW (G = 10), 3.3 mA/Amplifier, ± 2.4 V to ± 18 V, - 40 °C to 125 °C specified
ZJA3676/7	Low power, G = 1 Single/Dual 36 V difference amplifier	Input protection to ± 65 V, CMRR 104 dB min, Vos 100 µV max, gain error 15 ppm max, 500 kHz BW, 330 µA, 2.7 to 36 V
Precision Voltage Reference		
ZJR1000	15 V supply precision voltage reference	V_{OUT} = 1.25/2.048/2.5/3/4.096/5 V, 5 ppm/°C max drift - 40 °C to 125 °C, ± 0.05 % initial error
ZJR1001 ZJR1002 ZJR1003	5.5V low power voltage reference (ZJR1001 with noise filter option)	V_{OUT} = 2.5/3/4.096/5 V, 5 ppm/°C max drift - 40 °C to 125 °C, ± 0.05 % initial error, 130 µA, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MS-8
Switch and Multiplexer		
ZJG4438/4439	36V fault protection 8:1/dual 4:1 multiplexer	Protection to ± 50 V power on & off, latch-up immune, Ron 270 Ω, 14.8 pC charge injection, t_{ON} 166 nS, 10 V to 36 V